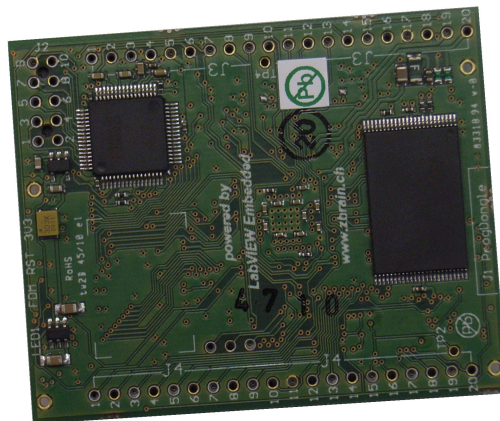


# Preliminary

# Z24-C1

# Z27-C1



# Mixed Signal Coremodules

## Hardware Manual

Issue date: 15.02.2011

Schmid Engineering AG, Mezikonnerstrasse 9 , 9542 Munchwilen

[www.schmid-engineering.ch](http://www.schmid-engineering.ch)

## Table of Contents

|  |    |
|--|----|
| 1 Imprint.....                             | 3  |
| 2 Introduction.....                        | 4  |
| 3 Key Features.....                        | 4  |
| 4 Block Diagram.....                       | 5  |
| 5 Programming Interface (Prog-Dongle)..... | 6  |
| 6 Dimensions.....                          | 7  |
| 7 Connector Overview.....                  | 8  |
| 8 Connector pin assignment.....            | 9  |
| 8.1 Legend.....                            | 9  |
| 8.2 Connector J3.....                      | 9  |
| 8.3 Connector J4.....                      | 10 |
| 8.4 Connector J2 (AINB, optional).....     | 10 |
| 9 Port & Signal Descriptions.....          | 11 |
| 10 Basic Application Example.....          | 13 |
| 11 Technical Data.....                     | 14 |
| 12 Ordering Information.....               | 15 |
| 13 Accessories.....                        | 15 |
| 14 Product Anomalies.....                  | 16 |
| 15 Product Changes.....                    | 16 |
| 16 Document Revision History.....          | 16 |
| 17 Contact Information.....                | 17 |

## 1 Imprint

Copyright © 2010 by Schmid Engineering AG. All rights reserved.

Schmid Engineering AG  
Mezikonerstrasse 9  
9542 Münchwilen  
Switzerland

email: [tech.support@schmid-engineering.ch](mailto:tech.support@schmid-engineering.ch)  
homepage: [www.schmid-engineering.ch](http://www.schmid-engineering.ch)  
Online Wiki: <http://wiki.schmid-engineering.ch>

**DISCLAIMER:** *Schmid Engineering AG disclaims any and all liability for the accuracy and completeness of the information contained in this publication as well as its suitability for any particular purpose. The user assumes responsibility for any and all consequences arising from the use of the information contained in this publication. Terms of delivery and rights of technical change reserved.*



**Warning:** *ESD (electrostatic discharge) sensitive device. Proper ESD handling required.*

## 2 Introduction

Z24-C1 and Z27-C1 are members of the *Zbrain-System product family*, powered by LabVIEW Embedded.

Z24-27-C1 are a mixed signal core modules, based on the powerfull ADSP-BF527/524 processor.

They feature 4 low range signal analog inputs and up to 8 analog inputs with industrial input range, high input impedance and over voltage protection, which allows for direct connection to real world signals without the need for external circuitry.

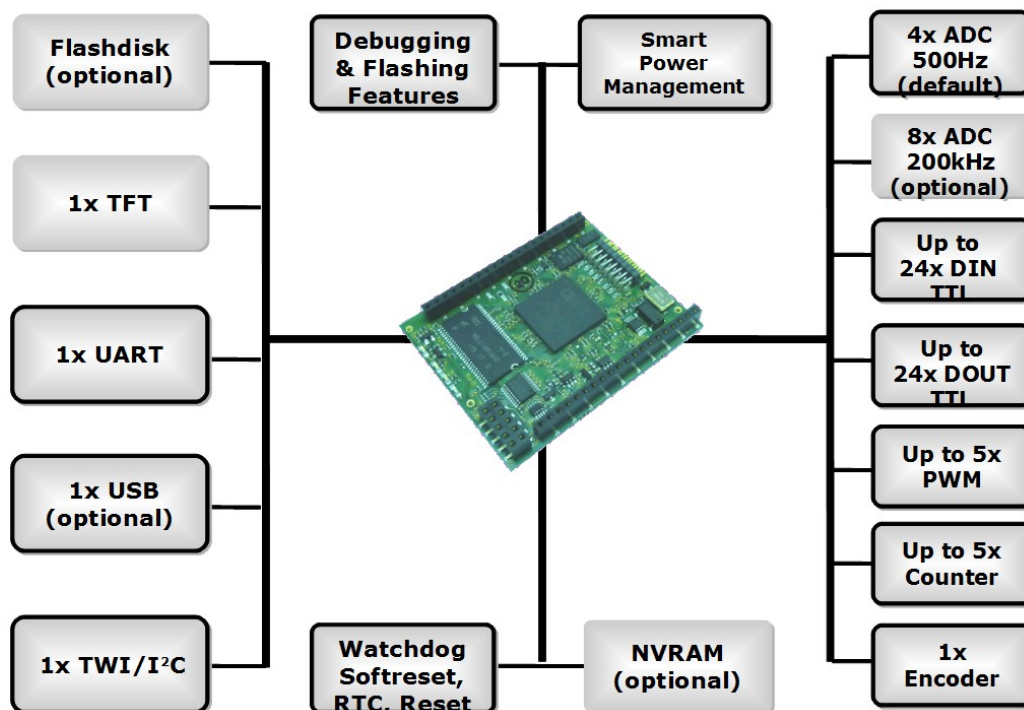
All *digital IO* signals are 3.3V TTL level and need to be driven on the base board.

Integration is very easy thanks to reliable 2.54mm pitch standard connectors, single 3.3V supply, and on board in programming interface.

## 3 Key Features

- Powered by LabVIEW Embedded (LabVIEW for Microprocessor)
- 400MHz ADSP-BF524/527 processor
- 256MByte on board flash disk (optional)
- 4x 0..3V analog inputs, 500Hz
- 8x +-5/+-10V industrial range analog inputs, protected and filtered (optional)
- up to 24 DIO (multiplexed with other functions)
- up to 5 Timer inputs / PWM outputs
- 1x rotary encoder interface
- 1x UART serial interface (e.g. for RS232, RS485, RS422)
- 1x TWI
- USB (optional)
- 16Bit LCD TFT interface (multiplexed with other functions)
- dynamic power management
- on board test points for analog and digital io

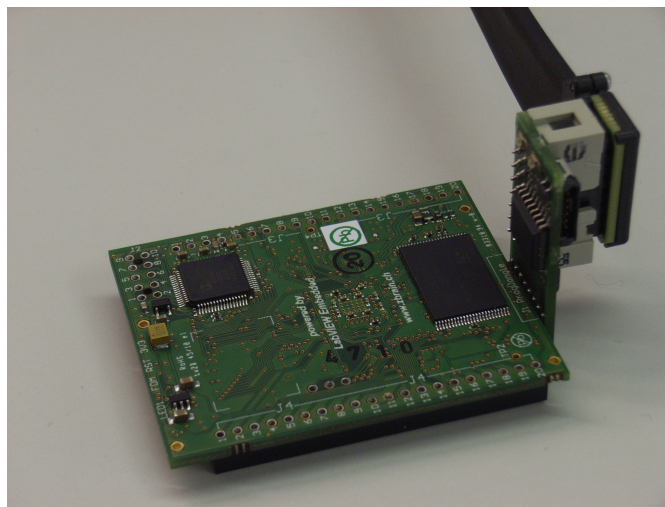
## 4 Block Diagram



## 5 Programming Interface (Prog-Dongle)

At delivery the fast Debug Mode (FDM) interpreter is pre flashed and indicates its activity by toggeling the FDM-LED. If the LED isn't toggeling, the FDM interpreter can be downloaded through the Emulator.

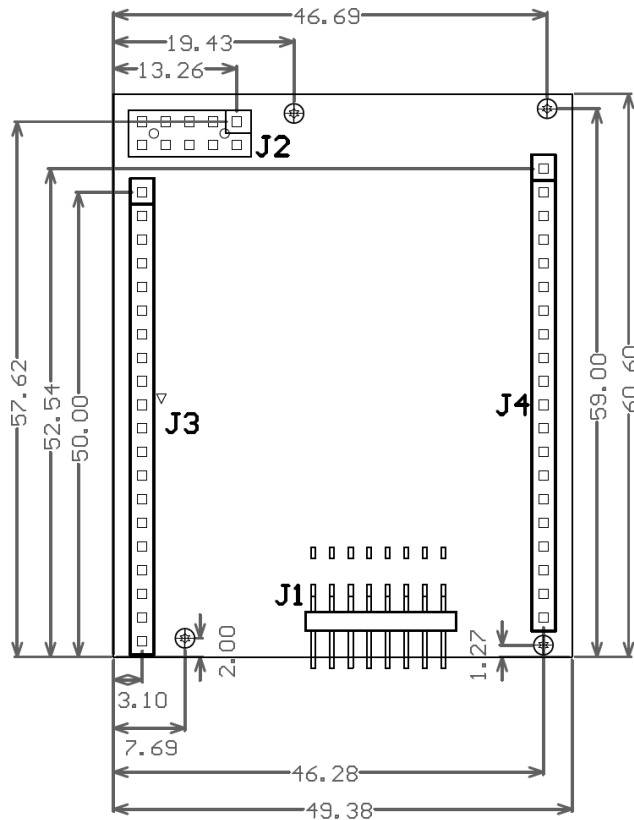
Z24-27-C1 feature a universal programming dongle (Prog-Dongle) for FDM programming, emulator connection, series production and field updates. This eliminates the need for any additional programming connectors on the base board.



**note:** reserve enough space on the baseboard to be able to plug the ProgDongle in and out.

## 6 Dimensions

### TOP VIEW:

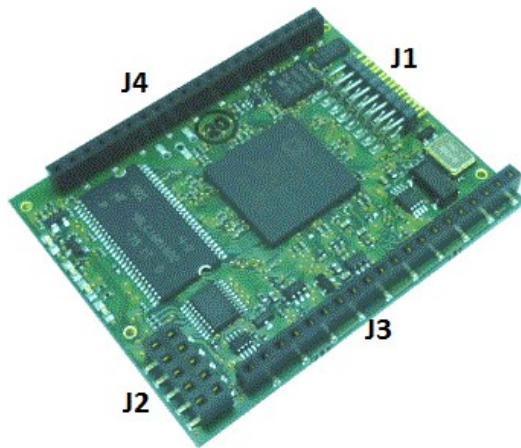


### Notes:

- **TOP VIEW**
- All connector positions are within a **2.54mm grid**, which allows for easy setups on vero boards
- instead of mounting holes the board provides 4 pads to solder the board onto the baseboard
- dimensions indicate connectors pin 1

## 7 Connector Overview

### BOTTOM - VIEW



J1 : Programming connector (ProgDongle)

J2 : Analog In [10pol]

J3 : Analog & Digital IO [20pol]

J4 : Digital IO [20pol]

J[2..4] are standard 2.54mm sockets with reliable two point contacts.

Recommended mating parts for baseboard connectors are any standard 2.54mm headers with gold plating, e.g. Multicomp MC34739 (farnell 1593423)



## 8 Connector pin assignment

### 8.1 Legend

|      |                             |      |                      |
|------|-----------------------------|------|----------------------|
| [I]  | = Input                     | pu   | = internal pull up   |
| [O]  | = Output                    | pd   | = internal pull down |
| [IO] | = Bidirectional             |      |                      |
| AIN  | = Analog Input              | DIO  | = Digital IO         |
| TMR  | = Timer Input or PWM output | ENC  | = Encoder input      |
| TWI  | = Two wire interface        | UART | = Serial interface   |
| USB  | = USB interface             | VRTC | = RTC backup input   |
| MR   | = Manual reset input        |      |                      |

#### Notes:

- **All pins are TTL 3.3V level, unless noted otherwise**  
( $I_{max} = 2mA$ , NOT short circuit protected, take special care when configuring pins as outputs,  $U_{oh} > 2.7V$ ,  $U_{ol} < 0.4V$ )
- **All pins except AINB and USB unprotected processor pins**
- **All inputs can be left open**

**All programmable IO pins are high impedance during power up and reset. They remain high impedance until defined otherwise by software.**

### 8.2 Connector J3

| Pin   | 1. Function  | 2. Function | 3. Function | notes   |
|-------|--------------|-------------|-------------|---|
| J3-1  | AINA-CH0 [I] |             |             | 0..3V, up to 500Hz                                |
| J3-2  | AINA-CH1 [I] |             |             | 0..3V, up to 500Hz                                |
| J3-3  | AINA-CH2 [I] |             |             | 0..3V, up to 500Hz                                |
| J3-4  | AINA-CH3 [I] |             |             | 0..3V, up to 500Hz                                |
| J3-5  | GND          |             |             |   |
| J3-6  | TWI SCL [O]  |             |             | pu 2k (only external pullup only to 3.3V allowed) |
| J3-7  | TWI SDA [IO] |             |             | pu 2k (only external pullup only to 3.3V allowed) |
| J3-8  | DIO16 [IO]   | TMR A [IO]  |             |   |
| J3-9  | DIO17 [IO]   | TMR B [IO]  |             |   |
| J3-10 | DIO18 [IO]   | TMR C [IO]  |             |   |
| J3-11 | DIO19 [IO]   |             |             |   |
| J3-12 | DIO20 [IO]   |             |             |   |
| J3-13 | DIO21 [IO]   |             |             |   |
| J3-14 | MR [I]       |             |             | pu 10k  |
| J3-15 | VRTC [I]     |             |             | 2.7..3.6V   |
| J3-16 | VCC (3.3V)   |             |             |   |
| J3-17 | GND          |             |             |   |
| J3-18 | USB VBUS     |             |             | optional  |
| J3-19 | USB D-       |             |             | optional  |
| J3-20 | USB D+       |             |             | optional  |

## 8.3 Connector J4

| Pin   | 1. Function | 2. Function     | 3. Function | Notes |
|-------|-------------|-----------------|-------------|-------|
| J4-1  |             |                 | LCD CLK     |       |
| J4-2  | DIO23 [IO]  | TMR E [IO]      | LCD FS1     |       |
| J4-3  | DIO22 [IO]  | TMR F [IO]      | LCD FS2     |       |
| J4-4  | DIO0 [IO]   |                 | LCD R0 [O]  |       |
| J4-5  | DIO1 [IO]   |                 | LCD R1 [O]  |       |
| J4-6  | DIO2 [IO]   |                 | LCD R2 [O]  |       |
| J4-7  | DIO3 [IO]   |                 | LCD R3 [O]  |       |
| J4-8  | DIO4 [IO]   |                 | LCD R4 [O]  |       |
| J4-9  | DIO5 [IO]   |                 | LCD G0 [O]  |       |
| J4-10 | DIO6 [IO]   |                 | LCD G1 [O]  |       |
| J4-11 | GND         |                 |             |       |
| J4-12 | DIO7 [IO]   |                 | LCD G2 [O]  |       |
| J4-13 | DIO8 [IO]   |                 | LCD G3 [O]  |       |
| J4-14 | DIO9 [IO]   | UART1 TXEN [O]  | LCD G4 [O]  |       |
| J4-15 | DIO10 [IO]  | UART1 /RXEN [O] | LCD G5 [O]  |       |
| J4-16 | DIO11 [IO]  | ENC CZM         | LCD B0 [O]  |       |
| J4-17 | DIO12 [IO]  | ENC CDG         | LCD B1 [O]  |       |
| J4-18 | DIO13 [IO]  | ENC CUD         | LCD B2 [O]  |       |
| J4-19 | DIO14 [IO]  | UART1 TX [O]    | LCD B3 [O]  |       |
| J4-20 | DIO15 [IO]  | UART1 RX [I]    | LCD B4 [O]  |       |

## 8.4 Connector J2 (AINB, optional)

| Pin   | Function/Name | notes  |
|-------|---------------|--|
| J2-1  | AINBGND [I]   | Analog Reference Potential, must be connected to GND or AGND |
| J2-2  | AINBGND [I]   | Analog Reference Potential, must be connected to GND or AGND |
| J2-3  | AINB-CH7 [I]  | +5V / +-10V Analog Input                                     |
| J2-4  | AINB-CH6 [I]  | +5V / +-10V Analog Input                                     |
| J2-5  | AINB-CH5 [I]  | +5V / +-10V Analog Input                                     |
| J2-6  | AINB-CH4 [I]  | +5V / +-10V Analog Input                                     |
| J2-7  | AINB-CH3 [I]  | +5V / +-10V Analog Input                                     |
| J2-8  | AINB-CH2 [I]  | +5V / +-10V Analog Input                                     |
| J2-9  | AINB-CH1 [I]  | +5V / +-10V Analog Input                                     |
| J2-10 | AINB-CH0 [I]  | +5V / +-10V Analog Input                                     |

## 9 Port & Signal Descriptions

**Note: All pins are TTL 3.3V level, unless specified otherwise**  
 (Imax = 2mA, NOT short circuit protected, direct processor pins)

| Description   | Specifications  |
|---|---|
| <p><b>AINA[0..3] Analog In Group A</b><br/>                     Analog Inputs for low performance applications<br/>                     Samplerate &lt; 500Hz</p> <p>This inputs are referenced to GND</p> <p>please note that the sample rate is influenced by devices connected to the TWI bus.</p>   | <p>0..3V<br/>                     10 Bit, 500Hz<br/>                     NOT OVP protected</p> <p>Input impedance typ 1M Ohm<br/>                     temperature stability +- typ 40 ppm/°C</p>  |
| <p><b>AINB[0..7] Analog In Group B (optional)</b><br/>                     Analog Inputs with a software selectable +-5V / +-10V input range<br/>                     Simultaneous Sampling of all 8 channels.<br/>                     Built in 2<sup>nd</sup> order analog anti aliasing filter (22kHz@-3dB)<br/>                     Software selectable digital filter options (down to 1.5kHz)<br/>                     Samplerate up to 200kHz (DMA)</p> <p><b>NOTE : AINBGND</b> is the reference potential for the analog inputs AINB[0..7].<br/> <b>AINBGND must be connected to GND or AGND on the baseboard.</b> It must have a potential similar to GND</p> | <p>+ -5V, + -10V<br/>                     16 Bit, simultaneous</p> <p>Input imp typ 1M Ohm<br/>                     OVP -15..+15V<br/>                     temperature stability +- 7ppm/°C<br/>                     No missing codes</p> |
| <p><b>DIO[0..23] Digital IO</b><br/>                     standard digital IO pins, direction software controlled</p>  | <p>3.3V TTL</p>   |
| <p><b>TMR[A..E] Timer Inputs and Outputs</b> (direction software controlled)<br/>                     PWM output, Measurement input and Counter capability</p>  | <p>TBD</p>  |
| <p><b>Encoder Interface</b><br/>                     Connects to a quadrature A/B signal encoders, optional with zero marker (ENC CMZ)</p>  |   |
| <p><b>TWI Two Wire Interface (I2C-interface)</b><br/>                     Standard TWI interface for easy IO extensions<br/>                     → <b>both signals need external pull up resistors (2k)</b></p>   | <p>typ 100kbps</p>  |
| <p><b>UART</b><br/>                     standard asynchronous serial interface supports e.g. RS232, RS485, RS422 or serial USB via FTDI<br/>                     -&gt; use RXEN/TXEN for RS485/422 driver control<br/>                     -&gt; NO RTS/CTS signals available</p>   | <p>up to 3Mbaud</p>   |
| <p><b>USB Interface (optional)</b><br/>                     slave only<br/>                     onboard protection circuits, connects directly to USB connectors on baseboard</p>   | <p>USB 1.0</p>  |

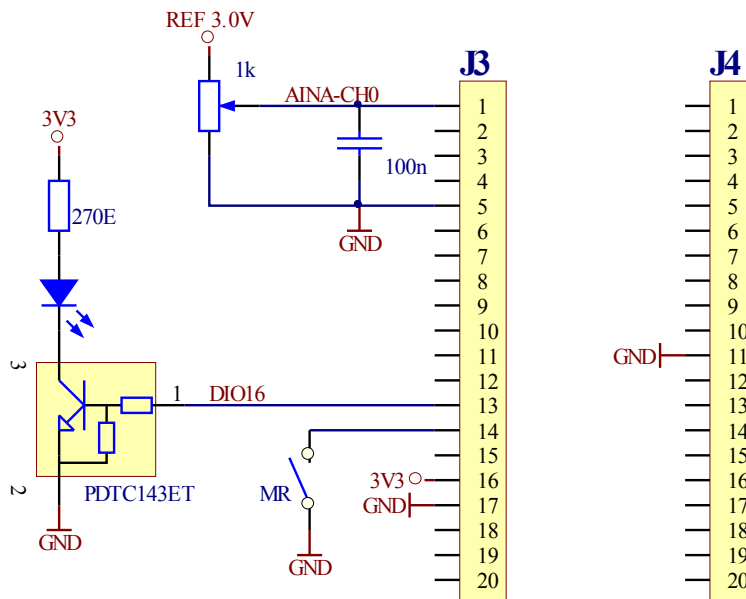
| Description  | Specifications                                   |
|--|--|
| <b>MR Manual Reset</b><br>active low external reset input. (optional)<br>integrated debouncer circuit<br>→ simply connect an reset button to GND if needed                                     | 40ms debounced                                   |
| <b>VRTC backup battery input</b><br>Backup voltage for internal real time clock. (VRTC keeps the internal RTC running, even if VCC is not present)<br>can be connected to a 3.6V LiIon battery | 2.7..3.6V<br>20uA typ                            |
| <b>VCC power supply input 3.3V</b><br>use a regulated 3.3V supply  | 3.3V / TBDA, +-5%<br>max 100mV p-to-p<br>0-20Mhz |
| <b>GND</b><br>→ please connect all GND pins to a GND plane on the base board   |  |

## 10 Basic Application Example

Integration into a custom baseboard is very easy. Just connect VCC (3.3V) to the board and the system is running and ready to go.

Add additional circuitry according to your needs.

In this basic example the Z48-C1 reads a potentiometer and controls an LED. The MR pushbutton allows to reset the board manually.



## 11 Technical Data

|                           |  |
|---------------------------|--|
| Dimensions                | 60.6 x 49.4mm                                    |
| Weight                    |  |
| Power Supply              | 3.3V, Typ. 0.5..2W (TBD)                         |
| Processor                 | ADSP-BF52x                                       |
| Memory                    | 8MByte SPI Bootflash, 32MB SDRAM 100Mhz, 2k FRAM |
| Temperature Range Ambient | -20..75°C  |
| Humidity                  | 10..90%, non condensing                          |
| ROHS                      | Compliant  |
| Warranty                  | 2 years product warranty                         |

## 12 Ordering Information

### Z2x-C1z

**[x = Processor Type]**

4 : ADSP-BF524 processor, 400MHz

7 : ADSP-BF527 processor, 500MHz

**[z = Assembly Option]**

A : full functionality

B : single sided, cost optimized

### Valid Ordering Codes:

| Ordering Code  | Processor | AINA          | AINB            | Flash disk | USB | Availability |
|----------------|-----------|---------------|-----------------|------------|-----|--------------|
| <b>Z27-C1A</b> | BF527     | 4x10Bit 500Hz | 8x14Bit, 200kHz | 256MB      | yes | Q1 2011      |
| <b>Z27-C1B</b> | BF527     | 4x10Bit 500Hz | -               | -          | no  | -            |
| <b>Z24-C1A</b> | BF524     | 4x10Bit 500Hz | 8x14Bit, 200kHz | 256MB      | yes | -            |
| <b>Z24-C1B</b> | BF524     | 4x10Bit 500Hz | -               | -          | no  | -            |

## 13 Accessories

| Picture | Ordering Code            | Description                         | Availability |
|---------|--------------------------|-------------------------------------|--------------|
|         | DEV-Z2X-C1               | Development Baseboard for Z24/27-C1 | Q1 2011      |
|         | ProgDongle_STD           | Programming Dongle                  | y            |
|         | RS232 DSUB adapter cable | RS232 DSUB adapter cable            | y            |
|         |                          |                                     |              |

## 14 Product Anomalies

| Version | Anomalies                                      |
|---------|--|
| V0.0    | ADCB supply incorrect, TWI tolerates only 3.3V |
|         |  |

## 15 Product Changes

| Version | Changes |
|---------|---------|
| V0.1    |         |
|         |         |

## 16 Document Revision History

| Date     | Vis. | Revision                             |
|----------|------|--------------------------------------|
| 30.12.09 | ab   | Preliminary release                  |
| 15.02.11 | ab   | Product Revision and Anomalies added |
|          |      |                                      |



## 17 Contact Information

Schmid Engineering AG  
Mezikonerstrasse 9  
CH-9542 Münchwilen  
Switzerland

email: [tech.support@schmid-engineering.ch](mailto:tech.support@schmid-engineering.ch)

homepage: [www.schmid-engineering.ch](http://www.schmid-engineering.ch)

Online Wiki: <http://wiki.schmid-engineering.ch>